

[Scope of Claim]

WHAT IS CLAIMED IS:

Please amend the claims as follows:

[Claim 1]

1. (Currently Amended) A method of manufacturing a semiconductor device-, comprising the steps:

~~a process of~~ forming a mask pattern on a laminate comprising a ~~lower~~ first conductive layer and ~~an upper~~ a second conductive layer;

~~a first etching process of~~ forming a first ~~conductive layer~~ pattern with a tapered sidewall portion ~~of~~ by etching the laminate;

performing a plasma treatment to be performed to the first ~~conductive layer~~ pattern with the tapered sidewall portion; and

~~a second etching process of~~ subjecting the first conductive layer pattern to anisotropic etching to form forming a second ~~conductive layer~~ pattern by anisotropic etching the first pattern with the tapered sidewall portion.

[Claim 2]

2. (Currently Amended) The method according to claim 1, wherein the plasma treatment is an argon plasma treatment.

[Claim 3]

3. (Currently Amended) The method according to claim 1, wherein a reaction product adhering to a the tapered sidewall portion ~~of the first conductive layer pattern~~ is removed by the performing the plasma treatment step.

[Claim 4]

4. (Currently Amended) The method according to claim 1, wherein the first conductive layer is made of a metal nitride.

[Claim 5]

5. (Currently Amended) A method of manufacturing a semiconductor device-, comprising the steps of:

~~a process of forming a mask pattern on a laminate comprising a lower first conductive layer and an upper a second conductive layer including titanium or including titanium as its main component;~~

~~a first etching process of forming a first conductive layer pattern with a tapered sidewall portion of~~ by etching the laminate;

~~performing a plasma treatment to be performed to the first conductive layer pattern with the tapered sidewall portion;~~ and

~~a second etching process of subjecting the first conductive layer pattern to anisotropic etching to form~~ forming a second conductive layer pattern by anisotropic etching the first pattern with the tapered sidewall portion.

[Claim 6]

6. (Currently Amended) The method according to claim 5, wherein the plasma treatment is an argon plasma treatment.

[Claim 7]

7. (Currently Amended) The method according to claim 5, wherein a reaction product adhering to a the tapered sidewall portion ~~of the first conductive layer pattern~~ is removed by the performing the plasma treatment step.

[Claim 8]

8. (Currently Amended) The method according to claim 5, wherein the first conductive layer is made of metal nitride.

[Claim 9]

9. (Currently Amended) A method of manufacturing a semiconductor device, comprising the steps of:

~~a process of forming a mask pattern on a laminate comprising a first conductive layer, a second conductive layer on the first conductive layer, and a third conductive layer on the second conductive layer;~~

~~a first etching process of forming a first conductive layer pattern with a tapered sidewall portion of by etching the laminate;~~

~~performing a plasma treatment to be performed to the first conductive layer pattern with the tapered sidewall portion; and~~

~~a second etching process of subjecting the first conductive layer pattern to anisotropic etching to form forming a second conductive layer pattern by anisotropic etching the first pattern with the tapered sidewall portion.~~

[Claim 10]

10. (Currently Amended) The method according to claim 5, wherein the plasma treatment is an argon plasma treatment.

[Claim 11]

11. (Currently Amended) The method according to claim 5, wherein a reaction product adhering to a the tapered sidewall portion ~~of the first conductive layer pattern~~ is removed by the performing the plasma treatment step.

[Claim 12]

12. (Currently Amended) The method according to claim 5, wherein the first conductive layer is made of a metal nitride.

[Claim 13]

13. (Currently Amended) The method according to claim 5, wherein the third conductive layer is made of a metal having high-melting point.

[Claim 14]

14. (Currently Amended) A method of manufacturing a semiconductor device-, comprising the steps of:

~~a process of forming a mask pattern on a laminate comprising a first conductive layer, a second conductive layer including titanium or including titanium as its main component on the first conductive layer-, and a third conductive layer on the second conductive layer;~~

~~a first etching process of forming a first conductive layer pattern with a tapered sidewall portion of~~ by etching the laminate;

~~performing a plasma treatment to be performed to the first conductive layer pattern;~~
with the tapered sidewall portion; and

~~a second etching process of subjecting the first conductive layer pattern to anisotropic etching to form~~ forming a second conductive layer pattern by anisotropic etching the first pattern with the tapered sidewall portion.

[Claim 15]

15. (Currently Amended) The method according to claim 14, wherein the plasma treatment is an argon plasma treatment.

[Claim 16]

16. (Currently Amended) The method according to claim 14, wherein a reaction product adhering to a the tapered sidewall portion ~~of the first conductive layer pattern~~ is removed by the performing the plasma treatment step.

[Claim 17]

17. (Currently Amended) The method according to claim 14, wherein the first conductive layer is made of a metal nitride.

[Claim 18]

18. (Currently Amended) The method according to claim 14, wherein the third conductive layer is made of a metal having high-melting point.

[Claim 19]

19. (Currently Amended) A method of manufacturing a semiconductor device-, comprising the steps of:

~~a process of forming a mask pattern on a laminate comprising a lower first conductive layer and an upper a second conductive layer over a semiconductor layer with a gate insulating film interposed therebetween;~~

~~a first etching process of forming a first conductive layer pattern with a tapered sidewall portion of by etching the laminate;~~

~~performing a plasma treatment to be performed to the first conductive layer pattern with the tapered sidewall portion;~~

~~a second etching process for subjecting the first conductive layer pattern to anisotropic etching to form forming a second conductive layer pattern by anisotropic etching the first pattern with the tapered sidewall portion; and~~

~~a process of adding an impurity elements to the semiconductor layer with the second conductive layer in the second conductive layer pattern as a shielding mask to form a region to which with the impurity elements is added in the semiconductor film,~~

~~which wherein the region with the impurity elements overlaps with the first conductive layer in the second conductive layer pattern.~~

[Claim 20]

20. (Currently Amended) The method according to claim 19, wherein the plasma treatment is an argon plasma treatment.

[Claim 21]

21. (Currently Amended) The method according to claim 19, wherein a reaction product adhering to a the tapered sidewall portion ~~of the first conductive layer pattern~~ is removed by the performing the plasma treatment step.

[Claim 22]

22. (Currently Amended) The method according to claim 19, wherein the first conductive layer is made of a metal nitride.

[~~Claim 23~~]

23. (Currently Amended) A method of manufacturing a semiconductor device, comprising the steps of:

~~a process of~~ forming a mask pattern on a laminate comprising a first conductive layer, a second conductive layer on the first conductive layer-, and a third conductive layer on the second conductive layer over a semiconductor layer with a gate insulating film interposed therebetween;

~~a first etching process of~~ forming a first conductive layer pattern with a tapered sidewall portion ~~of~~ by etching the laminate;

performing a plasma treatment ~~to be performed~~ to the first conductive layer pattern with the tapered sidewall portion;

~~a second etching process of~~ subjecting the first conductive layer pattern to anisotropic etching to form forming a second conductive layer pattern by anisotropic etching the first pattern with the tapered sidewall portion; and

~~a process of~~ adding an impurity elements to the semiconductor layer with the second conductive layer and the third conductive layer ~~in the second conductive layer pattern~~ as a shielding mask to form a region ~~to which~~ with the impurity elements ~~is added~~ in the semiconductor film,

~~which wherein~~ the region with the impurity elements overlaps with the first conductive layer ~~in the second conductive layer pattern~~.

[~~Claim 24~~]

24. (Currently Amended) The method according to claim 23, wherein the plasma treatment is an argon plasma treatment.

[~~Claim 25~~]

25. (Currently Amended) The method according to claim 23, wherein a reaction product adhering to a the tapered sidewall portion ~~of the first conductive layer pattern~~ is removed by the performing the plasma treatment step.

~~[Claim 26]~~

26. (Currently Amended) The method according to claim 23, wherein the first conductive layer is made of a metal nitride.

~~[Claim 27]~~

27. (Currently Amended) The method according to claim 23, wherein the third conductive layer is made of a metal having high-melting point.

~~[Claim 28]~~

28. (Currently Amended) A semiconductor device comprising a gate electrode comprising a lower first conductive layer and an upper second conductive layer including ~~titanium or including~~ titanium as its main component,

wherein a width of the first conductive layer is wider than ~~that~~ a width of the second conductive layer.

~~[Claim 29]~~

29. (Currently Amended) The semiconductor device according to clam ~~23~~ 28, wherein the lower first conductive layer is made of a metal nitride.

~~[Claim 30]~~

30. (Currently Amended) A semiconductor device comprising:
a gate electrode comprising a first conductive layer, a second conductive layer including titanium ~~or including titanium~~ as its main component on the first conductive layer-, and a third conductive layer on the second conductive layer,

wherein a width of the first conductive layer is wider than ~~these~~ a width of the second conductive layer and the third conductive layer.

~~[Claim 31]~~

31. (Currently Amended) The semiconductor device according to clam 30, wherein the first conductive layer is made of a metal nitride.

~~[Claim 32]~~

32. (Currently Amended) The semiconductor device according to clam 30, wherein the third conductive layer is made of a metal having high-melting point.

Please replace the abstract as provided on separate sheet: